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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/709,849

06/02/2004

Che-Li Lin

12920-US-PA

3848

31561

7590

12/05/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE

7 FLOOR-1, NO. 100

ROOSEVELT ROAD, SECTION 2

TAIPEI, 100

TAIWAN

EXAMINER

MOON, SEOKYUN

ART UNIT

PAPER NUMBER

2629

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,849	LIN, CHE-LI	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-17 is/are rejected.
- 7) ☒ Claim(s) 9 and 18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. The Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(a)-(d) has been acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo (US 2004/0227895) in view of Lee (US 2004/0085371).

As to **claim 1**, Yoo [drawing 1 provided on page 3 of this Office Action, which is equivalent to Yoo's figure 2] teaches a driving circuit (a combination of Yoo's gate drivers and source drivers) of a liquid crystal display, comprising:

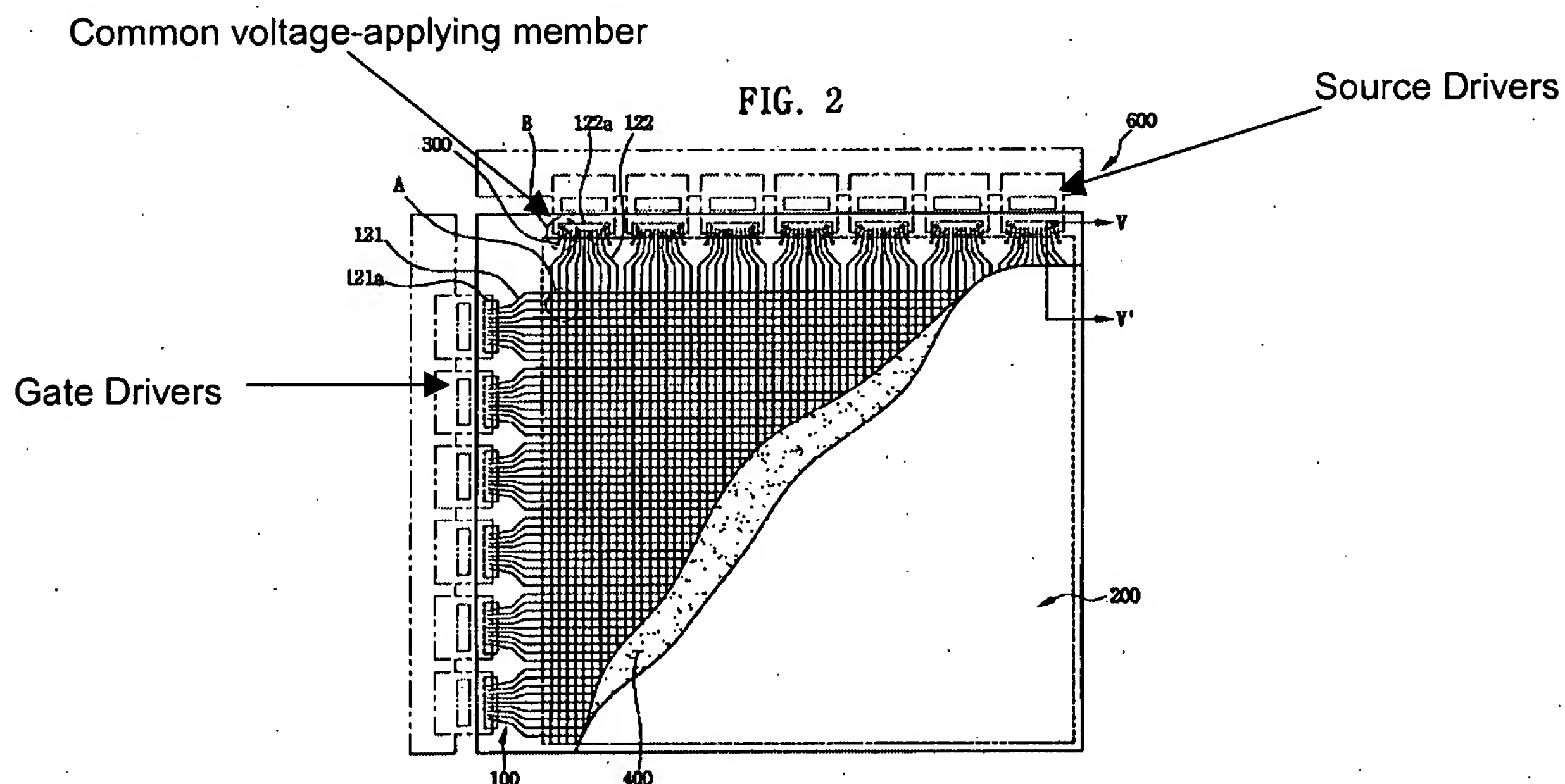
a plurality of gate drivers, for selectively driving a plurality of thin film transistors of the liquid crystal display [par. (0052) lines 6-10];

a plurality of source drivers, for receiving an image signal, the plurality of source drivers cooperating with the plurality of gate drivers to display an image on the liquid crystal display, each of the plurality of source drivers further comprising a common voltage generating circuit ("*common voltage-applying member 300*"), each of the common voltage generating circuit compensating, a common voltage output from each of the common voltage generating circuit to make each of the common voltage output from each of the common voltage generating circuit

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the same or to make each of the common voltage output to an ITO layer of a panel of the liquid crystal display the same [par. (0054) lines 6-10].

Yoo further inherently teaches a timing sequence controller, for providing a control signal (a signal controlling Yoo's gate drivers) and a data flow (a signal controlling Yoo's source drivers) to the plurality of gate drivers and the plurality of source drivers since it is required for Yoo to control the operation of the data drivers depending on the operation of the gate drivers so that the TFTs included in pixels of the display are turned on/off in appropriate timings to display images.



Drawing 1

Yoo does not teach the common voltage generating circuit to be capable of adjusting the outputted common voltage.

However, Lee [abstract] teaches a common voltage regulating circuit of a liquid crystal display from which the common voltages outputted are adjustable by software. Specifically, Lee

[fig. 15] teaches the common voltage regulating circuit outputting the common voltages based on a common voltage adjustable data ("*SDA*") and a clock signal ("*SCL*") [par. (0091)].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yoo's common voltage generating circuit to be adjustable, as taught by Lee, in order to provide Yoo's display a method of re-adjusting the common voltages fed to pixels of the display without using variable resistor, thus to allow fine adjustment and to reduce the manufacturing cost of the display [pars. (0013)-(0015)].

As to **claim 2**, Yoo modified by Lee teaches the adjustable common voltage generating circuit comprises [Lee: fig. 15]:

a digital interface (Lee: "*data storage section 500*"), for receiving the common voltage adjustable data (Lee: "*SDA*") and the clock signal (Lee: "*SCL*") [Lee: par. (0091)];

a digital to analog converter (Lee: "*D/A converter 502*"), coupled to the digital interface, for generating an analog signal based on the common voltage adjustable data (Lee: "*SDA*"); and an output buffer (Lee: "*buffer amplifying section 504*"), coupled to the digital to analog converter, for generating the common voltage based on the analog signal to drive a load of the common voltage.

As to **claim 3**, Yoo modified by Lee [Lee: fig. 15] teaches the digital interface comprises at least one of a serial digital interface (Lee: "*SDA*"), a parallel digital interface, a single-ended digital interface and a differential digital interface.

As to **claims 4 and 5**, Yoo modified by Lee [Lee: fig. 15] does not expressly disclose the internal structure / layout of the digital interface (Lee: "*data storage section 500*").

However, the Examiner takes official notice that it is well known in the art to use shift registers or latches to design and implement a digital data storage means.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify the modified Yoo's digital storage means to be implemented with shift register or latches since shift register and latches are well known for providing dynamic storages with low manufacturing cost.

As to **claim 6**, Yoo modified by Lee [Lee: fig. 15] teaches the output buffer (Lee: "*buffer amplifying section 504*") to comprise an operational amplifier (Lee: "*buffer amplifier 504a*").

As to **claim 7**, Yoo modified by Lee teaches the timing sequence controller to comprise a timing sequence control unit for providing the control signal and the data flow (Yoo: as discussed with respect to the rejection of claim 1) and a common voltage adjustable data generating unit (Lee: means for generating "*SDA*") for generating the common voltage adjustable data.

Yoo modified by Lee inherently teaches the timing sequence control unit and the common voltage adjustable data generating unit to be coupled since it is required for the modified Yoo to output the common voltages depending on the timing of providing gate voltages and source voltage to pixels in order to turn on/off the TFTs included in the pixels, thus to display images properly, and the timing sequence control unit and the common voltage adjustable data generating unit are required to be connected / coupled to each other in order to accomplish it.

As to **claim 8**, as discussed with respect to the rejection of claim 7, it is required for the modified Yoo's display to provide the control signal (the signals controlling the modified Yoo's gate drivers) and the data flow (the signals controlling the modified Yoo's source drivers) in accordance with the timings of outputting the common voltage adjustable data since it is required for the modified Yoo's display to provide the three driving signals (gate driving signals, source driving signals, and common electrode driving signals) in specific timings in order to turn

on/off the TFTs in pixels of the display in appropriate timings, thus to display images properly. Therefore, it is inherent for the modified Yoo's display that the operational sequence of the common voltage adjustable data generating unit (Lee: means for generating "SDA") to be controlled by the timing generating unit (Lee: means for generating the signals for controlling the gate drivers and the source drivers).

4. **Claims 10-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo and Lee as applied to claims 1-8 above, and further in view of Kim (US 2004/0113881).

As to **claim 10**, all of the claim limitations have already been discussed with respect to the rejection of claim 1 except for each of the plurality of the gate drivers comprising the adjustable common voltage generating circuit.

Yoo modified by Lee does not teach each of the plurality of the gate drivers to include a common voltage generating circuit.

However, Kim teaches a liquid crystal display adopting a method of supplying common voltages to display panel from gate printed circuits and source printed circuits.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yoo modified by Lee to include the adjustable common voltage generating circuits in each of the modified Yoo's plural gate drivers so that the common voltages are outputted from both of the plural gate drivers and the plural source drivers, as taught by Kim, in order to distribute the required wirings for common voltage electrodes uniformly on the display panel.

As to **claim 11**, all of the claim limitations have already been discussed with respect to the rejection of claim 2.

As to **claim 12**, all of the claim limitations have already been discussed with respect to the rejection of claim 3.

As to **claim 13**, all of the claim limitations have already been discussed with respect to the rejection of claim 4.

As to **claim 14**, all of the claim limitations have already been discussed with respect to the rejection of claim 5.

As to **claim 15**, all of the claim limitations have already been discussed with respect to the rejection of claim 6.

As to **claim 16**, all of the claim limitations have already been discussed with respect to the rejection of claim 7.

As to **claim 17**, all of the claim limitations have already been discussed with respect to the rejection of claim 8.

Allowable Subject Matter

5. **Claims 9 and 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ogawa (US 2004/0164943) teaches a liquid crystal device including a plurality of gate drivers wherein each of the plurality of gate drivers includes an adjustable common voltage generating circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 13, 2006

S.M.

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

